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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 09/592,230 | 06/12/2000 | Gregory Ralph Osborn | GEO4574 | 5504 |

7590

02/12/2003

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EXAMINER

MOORMAN, EARL J

ART UNIT

PAPER NUMBER

2683

DATE MAILED: 02/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/592,230

Applicant(s)

OSBORN, GREGORY RALPH

Examiner

Earl J. Moorman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) ____ is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). ____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

1. **Claims 14-16** are objected to because of the following informalities: It appears that claims 14-16 should be dependent upon independent claim 11 because of the antecedent basis of "a dynamic hardware resource investigation". However, they are written to depend on claim 1. With regards to the office action, the examiner's rejections are based on claims 14-16 being dependent upon independent claim 11. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-16** are rejected under 35 U.S.C. 102(b) as being anticipated by McVey et al. (U.S. Patent Number 5,479,477).

4. Regarding **claim 1**, McVey et al. teaches a method of characterizing hardware resource dependencies in a multi-channel communications system (abstract, col.3: lines

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4-28) comprising identifying constraints and interdependencies among hardware resources based on both stored system and queried hardware resource characteristics (col.4: lines 6-16, col.5: lines 43-46, col.6, lines 1-20) and generating an abstract resource specification based on the identifying of hardware resource constraints and interdependencies for use during hardware resource allocation to enable maximum preservation of most functional and least available hardware resources during hardware resource allocation (col.4: lines 62-67, col.5: lines 1-18, col.5: lines 43-67, col.7: lines 4-56).

5. Regarding **claim 2**, McVey et al. teaches a method wherein the identifying of constraints and interdependencies among hardware resources comprises identifying system communications domains that contain system hardware resources (col.3: lines 7-14, col.5: lines 46-67).

6. Regarding **claim 3**, McVey et al. teaches a method wherein the identifying of constraints and interdependencies among hardware resources comprises identifying managed hardware resources from among the system hardware resources (col.3: lines 43-51, col.4: lines 62-67, col.5: lines 1-18, col.5: lines 46-67).

7. Regarding **claim 4**, McVey et al. teaches a method wherein the identifying of constraints and interdependencies among hardware resources comprises identifying hardware resource groups and hardware resource group boundaries among the system hardware resources (col.3: lines 14-21, col.5: lines 46-67, col.7: lines 47-56).

8. Regarding **claim 5**, McVey et al. teaches a method wherein the identifying of constraints and interdependencies among hardware resources comprises assigning

association labels to the system hardware resources to identify relationships, if any, between the system hardware resources and external hardware (col.6: lines 48-65), to identify redundant resources within respective ones of the hardware resource groups, and to characterize dedicated coupling between individual ones of the system hardware resources (col. 5: lines 1-18, col.5: lines 46-67).

9. Regarding **claim 6**, McVey et al. also teaches a hardware resource identifier for a multi-channel communications system (FIG.1) comprising a hardware resource interdependency tracking device (which reads on identifying constraints and interdependencies among hardware resources) for recognizing constraints among available system hardware resources (col.3: lines 1-29), an association labeling device (which also reads on identifying constraints and interdependencies among hardware resources) for assigning association labels to certain of the system hardware resources having constraints identified by the hardware resource interdependency tracking device (col. 5: lines 1-18, col.5: lines 46-67) and a processor (FIG.1, numeral 123) for interpreting an abstract resource specification identifying the available system hardware resources and the constraints associated therewith in a manner that enables maximum preservation of most functional and least available hardware resources during hardware resource allocation (col.4: lines 62-67, col.5: lines 1-18, col.5: lines 43-67, col.7: lines 4-56).

10. Regarding **claim 7**, McVey et al. teaches a hardware resource identifier (FIG.1) further comprising a resource domain identifier (which reads on identifying system communications domains) for differentiating domains of system hardware resources for

use by the processor (FIG.1,numeral 123) in interpreting the abstract resource specification (abstract, col.3: lines 1-29, col.5: lines 46-67).

11. Regarding **claim 8**, McVey et al. also teaches the hardware resource identifier (FIG.1) further comprising a managed hardware resource identifier (which reads on identifying managed hardware resources) for identifying managed hardware resources from among the system hardware resources for use by the processor in interpreting the abstract resource specification (col.3: lines 43-51, col.4: lines 62-67, col.5: lines 1-18, col.5: lines 46-67).

12. Regarding **claim 9**, McVey et al. teaches the hardware resource identifier (FIG.1) further comprising a hardware resource group and group boundary identifier (which reads on identifying hardware resource groups and hardware resource group boundaries) for identifying hardware resource groups and group boundaries of the system hardware resources for use by the processor (FIG.1, numeral 123) in interpreting the abstract resource specification (col.3: lines 14-21, col.5: lines 46-67 col.7: lines 47-56).

13. Regarding **claim 10**, McVey et al. also teaches the hardware resource identifier (FIG.1) further comprising an association labeler (which reads on assigning labels to the system hardware resources) for assigning association labels to the system hardware resources to identify relationships, if any, between the system hardware resources and external hardware, to identify redundant hardware resources within respective ones of the hardware resource groups, and to characterize dedicated coupling between individual ones of the system hardware resources for use by the processor (FIG.1,

numeral 123) in interpreting the abstract resource specification (col. 5: lines 1-18, col.5: lines 46-67, col.7: lines 4-56).

14. Regarding **claim 11**, McVey et al. further teaches a method of characterizing a hardware topology of a software-defined communications system (abstract, col.3: lines 4-28) comprising querying a static system hardware specification to identify hardware resource constraints and interdependencies (col.4: lines 6-16, col.5: lines 43-46, col.6: lines 1-20), performing a dynamic hardware resource investigation to identify hardware resource constraints and interdependencies in addition to those identified during the querying of a static hardware specification (col. 3: lines 1-21) and interpreting an abstract hardware resource specification for use during hardware resource allocation to facilitate maximum preservation of most functional and least available hardware resources while still enabling application hardware resource needs to be met (col.4: lines 62-67, col.5: lines 1-18, col.5: lines 43-67, col.7: lines 4-56).

15. Regarding **claim 12**, McVey et al. teaches a method wherein the performing of a dynamic hardware resource investigation comprises interpreting an abstract hardware resource description including virtual hardware resource objects (application object descriptions) which identify application hardware requirements (abstract, col.5: lines 43-67), col.7: lines 47-56).

16. Regarding **claim 13**, McVey et al. also teaches a method wherein the performing of a dynamic hardware resource investigation comprises identifying system communications domains that contain system hardware resources (col.3: lines 7-14, col.5: lines 46-67).

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17. Regarding **claim 14**, McVey et al. also teaches a method wherein the performing of a dynamic hardware resource investigation comprises identifying system hardware resources that are managed hardware resources (col.3: lines 43-51, col.4: lines 62-67, col.5: lines 1-18, col.5: lines 46-67).

18. Regarding **claim 15**, McVey et al. also teaches a method wherein the performing of a dynamic hardware resource investigation comprises identifying hardware resource groups and hardware resource group boundaries among system hardware resources (col.3: lines 14-21, col.5: lines 46-67, col.7: lines 47-56).

19. Regarding **claim 16**, McVey et al. also teaches a method wherein the performing of a dynamic hardware resource investigation comprises assigning association labels to system hardware resources to identify relationships, if any, between the system hardware resources and external hardware, to identify redundant resources within respective ones of the hardware resource groups, and to characterize dedicated coupling between individual ones of the system hardware resources (col. 5: lines 1-18, col.5: lines 46-67).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Earl J. Moorman whose telephone number is (703) 305-8158.

The examiner can normally be reached on Monday-Friday 8:00am-4:30pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William G. Trost can be reached on (703) 308-5318. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-9508 for regular communications and (703) 305-9508 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Earl Moorman *EJM*
January 29, 2003

W. R.
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